



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Kenichi Satori

Confirmation No.: 9760

Application No.: 10/630,799

Art Unit: 2824

Filed: July 31, 2003

Examiner: Andrew Q. Tran

For: NONVOLATILE SEMICONDUCTOR
MEMORY DEVICE WITH ERROR
DETECTION AND CORRECTION CIRCUIT
(AS AMENDED)

Allowed: March 18, 2004

SUBMISSION OF CORRECTED FORMAL DRAWINGS

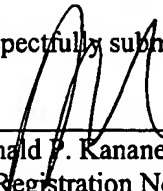
Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

We have enclosed corrected formal drawings in the above-identified application as required by the Examiner in the allowing papers of March 18, 2004.

Dated: June 17 2004

Respectfully submitted,

By 
Ronald P. Kananen

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